

SEP 21 2006

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IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend the claims to reflect the following:

Claims 1 – 55 (Canceled)

56. (Currently Amended) A delta-sigma modulator comprising:

a loop filter;

a comparator coupled to the loop filter; and

a switch, coupled to said comparator and said filter, said switch comprising:

first means for providing a first set of first and second complementary intermediate signals;

second means for providing a second set of third and fourth complementary intermediate signals;

third means responsive to the first set of signals for providing complementary output signals;

fourth means responsive to the second set of signals for providing complementary output signals; and

fifth means for selectively activating the third means or the fourth means in response to a control signal to switch signals from said filter in response to signals from said comparator clocking said first means and said second means to apply said first set of signals to said third means on a first edge of a clock pulse and apply said second set of signals to said fourth means on a second edge of said clock pulse.

57. (Original) The invention of Claim 56 wherein the first means is a master latch.

58. (Original) The invention of Claim 57 wherein the second means is a slave latch.

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59. (Original) The invention of Claim 58 wherein the slave latch has inputs provided by the master latch.

60. (Original) The invention of Claim 56 wherein the third means includes a first differential pair of transistors.

61. (Original) The invention of Claim 60 wherein the first differential pair of transistors includes first and second transistors Q1 and Q2, respectively.

62. (Previously Presented) The invention of Claim 61 wherein the first and second transistors are NPN transistors, for N-type semiconductor material and P-type semiconductor material.

63. (Original) The invention of Claim 62 wherein the first and second transistors are connected in a common emitter configuration.

64. (Previously Presented) The invention of Claim 61 wherein the first and second transistors are PNP transistors, for N-type semiconductor material and P-type semiconductor material.

65. (Original) The invention of Claim 61 wherein the first and second transistors are field effect transistors.

66. (Previously Presented) The invention of Claim 61 wherein a first intermediate signal is provided as an input to the first transistor and a second intermediate signal is provided as an input to the second transistor.

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67. (Original) The invention of Claim 61 wherein the fourth means includes a second differential pair of transistors.

68. (Original) The invention of Claim 67 wherein the second differential pair of transistors includes third and fourth transistors Q3 and Q4, respectively.

69. (Previously Presented) The invention of Claim 68 wherein the third and fourth transistors are NPN transistors, for N-type semiconductor material and P-type semiconductor material.

70. (Original) The invention of Claim 69 wherein the third and fourth transistors are connected in a common emitter configuration.

71. (Previously Presented) The invention of Claim 68 wherein the third and fourth transistors are PNP transistors, for N-type semiconductor material and P-type semiconductor material.

72. (Original) The invention of Claim 68 wherein the third and fourth transistors are field effect transistors.

73. (Previously Presented) The invention of Claim 68 wherein a third intermediate signal is provided as an input to the third transistor and a fourth intermediate signal is provided as an input to the fourth transistor.

74. (Original) The invention of Claim 67 wherein the fifth means includes a third differential pair of transistors.

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75. (Original) The invention of Claim 74 wherein the fifth means includes fifth and sixth transistors Q5 and Q6 respectively.

76. (Previously Presented) The invention of Claim 75 wherein the fifth and sixth transistors are NPN transistors, for N-type semiconductor material and P-type semiconductor material.

77. (Original) The invention of Claim 76 wherein the fifth and sixth transistors are connected in a common emitter configuration.

78. (Previously Presented) The invention of Claim 75 wherein the fifth and sixth transistors are PNP transistors, for N-type semiconductor material and P-type semiconductor material.

79. (Original) The invention of Claim 75 wherein the fifth and sixth transistors are field effect transistors.

80. (Original) The invention of Claim 75 wherein inputs to the fifth and sixth transistors are provided by complementary clock signals.

81. (Previously Presented) The invention of Claim 80 wherein the fifth and sixth transistors have a terminal connected to a source and a terminal connected to one of the first and the second differential pair.

82. (Original) The invention of Claim 81 wherein the source is a current source.

83. (Original) The invention of Claim 82 wherein the source is a cascode current source.

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84. (Canceled)

85. (New) A delta-sigma modulator comprising:

a loop filter;

a comparator coupled to the loop filter;

a master latch coupled to said comparator for providing a first set of first and second complementary intermediate signals;

a slave latch coupled to said master latch for providing a second set of third and fourth complementary intermediate signals;

a first differential pair of transistors responsive to the first set of signals for providing a first set of complementary output signals;

a second differential pair of transistors responsive to the second set of signals for providing a second set of complementary output signals; and

fifth means for switching current through said first differential pair of transistors and said second differential pair of transistors after the inputs thereof have settled to a full logic value.

86. (New) The invention of claim 85 wherein the first differential pair of transistors includes first and second transistors Q1 and Q2, respectively.

87. (New) The invention of claim 86 wherein the first and second transistors are NPN transistors, for N-type semiconductor material and P-type semiconductor material.

88. (New) The invention of claim 87 wherein the first and second transistors are connected in a common emitter configuration.

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89. (New) The invention of claim 86 wherein the first and second transistors are PNP transistors, for N-type semiconductor material and P-type semiconductor material.

90. (New) The invention of claim 86 wherein the first and second transistors are field effect transistors.

91. (New) The invention of claim 86 wherein a first intermediate signal is provided as an input to the first transistor and a second intermediate signal is provided as an input to the second transistor.

92. (New) The invention of claim 86 wherein the fourth means includes a second differential pair of transistors.

93. (New) The invention of claim 92 wherein the second differential pair of transistors includes third and fourth transistors Q3 and Q4, respectively.

94. (New) The invention of claim 93 wherein the third and fourth transistors are NPN transistors, for N-type semiconductor material and P-type semiconductor material.

95. (New) The invention of claim 94 wherein the third and fourth transistors are connected in a common emitter configuration.

96. (New) The invention of claim 93 wherein the third and fourth transistors are PNP transistors, for N-type semiconductor material and P-type semiconductor material.

97. (New) The invention of claim 93 wherein the third and fourth transistors are field effect transistors.

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98. (New) The invention of claim 93 wherein a third intermediate signal is provided as an input to the third transistor and a fourth intermediate signal is provided as an input to the fourth transistor.

99. (New) The invention of claim 92 wherein the fifth means includes a third differential pair of transistors.

100. (New) The invention of claim 99 wherein the fifth means includes fifth and sixth transistors Q5 and Q6 respectively.

101. (New) The invention of claim 100 wherein the fifth and sixth transistors are NPN transistors, for N-type semiconductor material and P-type semiconductor material.

102. (New) The invention of claim 101 wherein the fifth and sixth transistors are connected in a common emitter configuration.

103. (New) The invention of claim 100 wherein the fifth and sixth transistors are PNP transistors, for N-type semiconductor material and P-type semiconductor material.

104. (New) The invention of claim 100 wherein the fifth and sixth transistors are field effect transistors.

105. (New) The invention of claim 100 wherein inputs to the fifth and sixth transistors are provided by complementary clock signals.

106. (New) The invention of claim 100 wherein the fifth and sixth transistors have a terminal connected to a source and a terminal connected to one of the first and the second differential pair.

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107. (New) The invention of claim 106 wherein the source is a current source.

108. (New) The invention of claim 107 wherein the source is a cascode current source.